Instrução de Multiplicação (MUL)

Especificado por: Fluxo geral, fluxo detalhado e máquina de estado em Verilog.

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1. Introdução

Analisando a arquitetura e instruções do processador PD8 fornecido, é implementado uma instrução de multiplicação para este processador, sendo necessário um registrador extra que funciona apenas como armazenamento, este registrador é referido como ACC e seu sinal de saída LACC.

Este documento descreve o fluxo geral, o fluxo detalhado e uma máquina de estado em verilog para este processador.

1. Fluxo Geral

MAH <- M[PC]

PC <- PC + 1

MAL <- M[PC]

PC <- PC + 1

MD <- M[MA]

AC <- MD

M[SP] <- RFLAGS

SP <- SP - 1

Push

Accumulator

M[SP] <- AC

SP <- SP - 1

-----AQUI-----

MD <- AC

AC <- AC + MD

MD <- MDL

AC <- SHR(AC)

AC <- SHR(AC)

MD <- AC

SP <- SP + 1

AC <- M[SP]

SP <- SP + 1

RFLAGS <- M[SP]

Pop Accumulator

AC <- MDH

AC <- SHR(AC)

AC <- SHR(AC)

AC < 1

0 1

MD < 1

0 1

AC <- MD

AC < MD

0 1

ACC <- MD

MD <- AC

ACC <- AC

MD < 2

0 1

M[SP] <- AC

M[SP] <- RFLAGS

SP <- SP - 1

SP <- SP - 1

Push

Accumulator

AC <- MD

MD <- ACC

ACC<- AC

AC <- M[SP]

SP <- SP + 1

RFLAGS <- M[SP]

SP <- SP + 1

POP

AC <- AC + MD

M[SP] <- RFLAGS

SP <- SP - 1

M[SP] <- AC

SP <- SP - 1

PUSH

AC <- ACC

ACC <- MD

AC <- AC - MD

MD<- 1

DEC

MD <- AC

RFLAGS <- M[SP]

AC <- M[SP]

SP <- SP + 1

SP <- SP + 1

Pop Accumulator

1. Fluxo Detalhado

T4

ENPCA

T5

ENPCA

MR

ENPCA

MR

(LMAH)

T6

T7

(INCPC)

T8

ENPCA

ENPCA

MR

(LMAL)

ENPCA

MR

T9

T10

T11

(INCPC)

ENMAA

ENMAA

MR

T12

T13

ENMAA

MR

(LMD)

ENDES

(LAC)

T14

T15

ENSPA

ENFLD

ENSPA

ENFLD

MW

T16

(DECSP)

T17

ENSPA

ENDES

T18

ENSPA

ENDES

MW

T19

(DECSP)

(LRESET)

(LINT)

T20

ENDES

(LMD)

T21

T22

ENDES

OP2

(LAC)

(LRESET)

(LINT)

ENDES

(LMD)

ENDES

OP2

(LAC)

(LRESET)

(LINT)

T23

T24

ENDES

(LMD)

ENDES

OP2

(LAC)

(LRESET)

(LINT)

ENDES

(LMD)

ENDES

OP2

(LAC)

(LRESET)

(LINT)

T25

T26

T27

T28

T29

ENDES

SD0

(LAC)

(LRESET)

(LINT)

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T30

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T31

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T32

ENDES

(LMD)

T33

(INCSP)

T34

T35

ENSPA

ENSPA

MR

(LAC)

ENSPA

MR

T36

T37

ENSPA

MR

ENSPA

(INCSP)

T38

T39

T40

T41

ENSPA

MR

(LINTE)

(LCARRY)

(LZERO)

(LRESET)

(LINT)

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T42

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T43

T44

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T45

ENDES

SD0

(LAC)

(LRESET)

(LINT)

AC < 1

MD < 1

ENDES

LAC

T46

T0

AC < MD

ENDES

LACC

ENDES

LACC

47

48

ENDES

(LMD)

MD < 2

T49

(DECSP)

ENSPA

ENDES

ENSPA

ENDES

MW

(DECSP)

(LRESET)

(LINT)

ENSPA

ENFLD

ENSPA

ENFLD

MW

T50

T51

T52

T53

T54

ENDES

LAC

T55

T56

ENDES

(LMD)

ENDES

LAAC

T57

ENSPA

MR

(INCSP)

ENSPA

MR

(LAC)

ENSPA

T58

T59

T60

T61

(INCSP)

T62

T63

ENSPA

ENSPA

MR

T64

T65

ENSPA

MR

(LINTE)

(LCARRY)

(LZERO)

(LRESET)

(LINT)

T66

ENDES

OP2

(LAC)

(LRESET)

(LINT)

ENSPA

ENFLD

T67

T68

ENSPA

ENFLD

MW

(DECSP)

ENSPA

ENDES

ENSPA

ENDES

MW

(DECSP)

(LRESET)

(LINT)

T69

T70

T71

T72

T73

ENDES

LAC

ENDES

(LAAC)

T74

ENCA

CON

(LMD)

N

LAC

T75

ENDES

OP2

OP1

(LAC)

T76

T77

ENDES

(LMD)

(INCSP)

ENSPA

ENSPA

MR

ENSPA

MR

ENSPA

MR

(LAC)

(INCSP)

ENSPA

T78

T79

T80

T81

T82

T83

T84

T85

ENSPA

MR

(LINTE)

(LCARRY)

(LZERO)

(LRESET)

(LINT)

1. Máquina de Estados

module mulMachine(clock, SIGNAL);

reg [32:0] T;

input clock;

output SIGNAL;

//reseta o sinais para a borda de descida

always @(negedge clock)

begin

ENPCA = 0;

MR = 1;

LMAH = 0;

LMAL = 0;

INCPC = 0;

ENMAA = 0;

LMD = 0;

DECSP = 0;

ENDES = 0;

LAC = 0;

LMD = 0;

LAAC = 0;

LINT = 0;

LINTE = 0;

LRESET = 0;

SD0 = 0;

OP1 = 0;

OP2 = 0;

ENSPA = 0;

end

//Os sinais do processador são setados na borda de subida

always @(posedge clock)

case (T)

4: begin

ENPCA = 1;

T = 5;

end

5: begin

ENPCA = 1;

MR = 0;

T = 6;

end

6: begin

ENPCA = 1;

MR = 0;

LMAH = 1;

T = 7;

end

7: begin

INCPC = 1;

T = 8;

end

8: begin

ENPCA = 1;

T = 9;

End

9: begin

ENPCA = 1;

MR = 0;

T = 10;

end

10: begin

ENPCA = 1;

MR = 0;

LMAL = 1;

T = 11;

end

11: begin

INCPC = 1;

ENMAA = 1;

T = 12;

end

12: begin

ENMAA = 1;

MR = 0;

T = 13;

end

13: begin

ENMAA = 1;

MR = 0;

LMD = 1;

T = 14;

end

14: begin

ENDES = 1;

LAC = 1;

T = 15;

end

15: begin

ENSPA = 1;

ENFLD = 1;

T = 16;

end

16: begin

ENSPA = 1;

ENFLD = 1;

MW = 0;

T = 17;

end

17: begin

DECSP = 1;

T = 18;

end

18: begin

ENSPA = 1;

ENDES = 1;

T = 19;

end

19: begin

ENSPA = 1;

ENDES = 1;

MW = 0;

T = 20;

End

20: begin

DECSP = 1;

LRESET = 1;

LINT = 1;

T = 21;

end

21: begin

ENDES = 1;

LMD = 1;

T = 22;

end

22: begin

ENDES = 1;

OP2 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 25;

end

23: begin

ENDES = 1;

LMD = 1;

T = 24;

End

24: begin

ENDES = 1;

OP2 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 25;

end

25: begin

ENDES = 1;

LMD = 1;

T = 26;

end

26: begin

ENDES = 1;

OP2 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 27;

end

27: begin

ENDES = 1;

LMD = 1;

T = 28;

end

28: begin

ENDES = 1;

OP2 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 29;

end

29: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 30;

end

30: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 31;

End

31: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 32;

end

32: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 33;

end

33: begin

ENDES = 1;

LMD = 1;

T = 34;

end

34: begin

INCSP = 1;

T = 35;

end

35: begin

ENSPA = 1;

T = 36;

End

36: begin

ENSPA = 1;

MR = 0;

T = 37;

end

37: begin

ENSPA = 1;

MR = 0;

LAC = 1;

T = 38;

end

38: begin

INCSP = 1;

T = 39;

end

39: begin

ENSPA = 1;

T = 40;

end

40: begin

ENSPA = 1;

MR = 0;

T = 41;

End

41: begin

ENSPA = 1;

MR = 0;

LINTE = 1;

LCARRY = 1;

LZERO = 1;

LRESET = 1;

LINT = 1;

T = 42;

end

42: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 43;

end

43: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 44;

End

44: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 45;

end

45:begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

if(AC<1)

begin

A = 1;

T = 0;

end

else

if (MD < 1)

begin

T = 46;

end

else

begin

T = 47;

end

end

46:begin

ENDES = 1;

LACC = 1;

A = 1;

T = 0;

47:begin

ENDES = 1;

LACC = 1;

if(AC<MD)

T = 48;

else

T = 49;

end

48:begin

ENDES = 1;

LMD = 1;

T = 49;

end

49:begin

if(MD<2)

begin

A = 1;

T = 0;

end

else

begin

ENSPA = 1;

ENFLD = 1;

end

T = 50;

End

50:begin

ENSPA = 1;

ENFLD = 1;

MW = 0;

T = 51;

end

51:begin

DECSP = 1;

T = 52;

end

52:begin

ENSPA = 1;

ENDES = 1;

T = 53;

end

53:begin

ENSPA = 1;

ENDES = 1;

MW = 0;

T = 54;

end

54: begin

DECSP = 1;

LRESET = 1;

LINT = 1;

T = 55;

End

55:begin

ENDES = 1;

LAC = 1;

T = 56;

end

56:begin

ENDES = 1;

LMD = 1;

T = 57;

end

57:begin

ENDES = 1;

LAAC = 1;

T = 58;

end

58:begin

INCPC = 1;

T = 59;

end

59:begin

ENSPA = 1;

T = 60;

end

60:begin

ENSPA = 1;

MR = 0;

T = 61;

End

61:begin

ENSPA = 1;

MR = 0;

LAC = 1;

T = 62;

end

62:begin

INCSP = 1;

T = 63;

end

63:begin

ENSPA = 1;

T = 64;

End

64:begin

ENSPA = 1;

MR = 0;

T = 65;

End

65: begin

ENSPA = 1;

MR = 0;

LINTE = 1;

LCARRY = 1;

LZERO = 1;

LRESET = 1;

LINT = 1;

T = 66;

end

66:begin

ENDES = 1;

OP2 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 67;

end

67:begin

ENSPA = 1;

ENFLD = 1;

T = 68;

End

68:begin

ENSPA = 1;

ENFLD = 1;

MW = 0;

T = 69;

end

69:begin

DECSP = 1;

T = 70;

end

70:begin

ENSPA = 1;

ENDES = 1;

T = 71;

end

71:begin

ENSPA = 1;

ENDES = 1;

MW = 0;

T = 72;

end

72:begin

DECSP = 1;

LRESET = 1;

LINT = 1;

T = 73;

end

73:begin

ENDES = 1;

LAC = 1;

T = 74;

end

74:begin

ENDES = 1;

LAAC = 1;

T = 75;

end

75:begin

ENCA = 1;

CON = 1;

LMD = 1;

T = 76;

End

76:begin

ENDES = 1;

OP2 = 1;

OP1 = 1;

LAC = 1;

T = 77;

end

77:begin

ENDES = 1;

LMD = 1;

T = 78;

end

78:begin

INCSP = 1;

T = 79

end

79:begin

ENSPA = 1;

T = 80;

end

81:begin

ENSPA = 1;

MR = 0;

T = 81;

end

81:begin

ENSPA = 1;

MR = 0;

LAC = 0;

T = 82;

End

82:begin

INCSP = 1;

T = 83;

end

83:begin

ENSPA = 1;

T = 84;

end

84:begin

ENSPA = 1;

MR = 0;

T = 85;

end

85:begin

ENSPA = 1;

MR = 0;

LINTE = 1;

LRESET = 1;

LCARRY = 1;

LINT = 1;

LZERO = 1;

T = 49;

end

default:

T = 0;

endcase

endmodule